WHAT IS CLAIMED IS:

1.   An encoder to encode a communication signal, comprising:

a signal buffer to buffer data associated with the communication signal;

a DC-Check circuit to compute a metric as a function of the data;

a DC tracking block to generate a flip signal as a function of the metric, the flip signal having a flip state and a nonflip state; and

a flip unit, responsive to the flip signal, to control a flip bit of an output of the signal buffer such that an average DC value of the data approaches zero.

2.   The encoder of Claim 1 wherein the metric is selected from a group consisting of a maximum absolute value of a running digital sum of the data, a maximum DC offset introduced by a filtering operation, a maximum DC offset of a DC correction circuit, a maximum absolute value of a filtered output of the data, a maximum DC offset slope change of the running digital sum of the data, a count of the quantity of times the metric is above or below a threshold, and combinations thereof.

3. The encoder of Claim 1 further comprising a precoder to generate the data from the communication signal.

4. The encoder of Claim 1 wherein the data includes sectors; and

the metric being a function of the data sectors.

5. The encoder of Claim 1 wherein the data includes codewords; and

the metric being a function of the data codewords.

6. The encoder of Claim 1 wherein the data includes past encoder outputs and possible future encoder outputs.

7. The encoder of Claim 1 wherein the flip bit is at least two flip bits.

8. The encoder of Claim 1 wherein the flip bit is inserted after every k input bits of the data.

9. The encoder of Claim 1 wherein there are two DC-Check circuits corresponding to each flip bit.

10. The encoder of Claim 1 wherein the DC-Check circuit includes limiting a maximum of an absolute value of a running digital sum.

11. The encoder of Claim 10 wherein the running digital sum up to time n is defined as;

$$RDS(T_0, n) = \sum_{i=T_0}^{n}(2x_i - 1), where(-\infty < T_0 < 0),$$

RDS(T_0,n) =RDS(T_o,-1)+RDS(0,n) and,

RDS0=RDS(T_o,-1),

where x_i represents encoder outputs, and RDS0 is a state of the DC-Check circuit before new data is entered.

12. The encoder of Claim 11 wherein an output of the DC-Check circuit for an input sequence of the data is;

$$RDS\max = \frac{\max}{0 \le n \le k}\left(\left|\sum_{i=0}^{n}(2x_i - 1) + RDS0\right|\right),$$

wherein the flip bit is inserted after k input bits.

13. The encoder of Claim 1 wherein the DC-Check circuit includes limiting a maximum DC offset of a filtering operation.

14. The encoder of Claim 13 wherein the DC-Check circuit includes a low pass filter having a transfer function that complements the filtering operation; and

an absolute value determiner to determine an absolute value of an output of the low pass filter.

15. The encoder of Claim 1 wherein the DC-Check circuit includes limiting for a DC correction circuit.

16. The encoder of Claim 15 wherein the DC-Check circuit includes a low pass filter to model the DC correction circuit; and

an offset estimation filter.

17. The encoder of Claim 1 wherein the DC-Check circuit includes threshold limiting.

18. A disk drive comprising:

a signal processor to process a perpendicular recording input signal;

a DC-free encoder to generate an encoded signal as a function of the perpendicular recording input signal, the DC-free encoder including;

a signal buffer to buffer data associated with the perpendicular recording input signal;

a DC-Check circuit to compute a metric as a function of the data;

a DC tracking block to generate a flip signal as a function of the metric, the flip signal having a flip state and a nonflip state; and

a flip unit, responsive to the flip signal, to control a flip bit of an output of the signal buffer such that an average DC value of the data approaches zero;

a preamplifier to transmit the encoded signal; and

media to store the encoded signal as first data.

19. The disk drive of Claim 18 further including a read head amplifier to read the first data from the media;

a DC-free decoder to decode the first data; and

the signal processor to generate an output signal as a function of the decoded first data.

20. The disk drive of Claim 19 wherein the metric is selected from a group consisting of a maximum absolute value of a running digital sum of the data, a maximum DC offset introduced by a filtering operation, a maximum DC offset of a DC correction circuit, a maximum absolute value of a filtered

output of the data, a maximum DC offset slope change of the

running digital sum of the data, a count of the quantity of

times the metric is above or below a threshold, and

combinations thereof.

21.   The disk drive of Claim 19 further comprising a

precoder to generate the data from the communication signal.

22.   The disk drive of Claim 19 wherein the data includes

sectors; and

the metric being a function of the data sectors.

23.   The disk drive of Claim 19 wherein the data includes

codewords; and

the metric being a function of the data codewords.

24.   The disk drive of Claim 19 wherein the data includes

past encoder outputs and possible future encoder outputs.

25.   The disk drive of Claim 19 wherein the flip bit is

at least two flip bits.

26.   The disk drive of Claim 19 wherein the flip bit is

inserted after every k input bits of the data.

27. The disk drive of Claim 19 wherein there are two DC-Check circuits corresponding to each flip bit.

28. The disk drive of Claim 19 wherein the DC-Check circuit includes limiting a maximum of an absolute value of a running digital sum.

29. The disk drive of Claim 28 wherein the running digital sum up to time n is defined as;

$$RDS(T_0, n) = \sum_{i=T_0}^{n} (2x_i - 1), where (-\infty < T_0 < 0),$$

RDS(T_0,n)=RDS(T_o,-1)+RDS(0,n) and,

RDS0=RDS(T_o,-1),

where x_i represents encoder outputs, and RDS0 is a state of the DC-Check circuit before new data is entered.

30. The disk drive of Claim 29 wherein an output of the DC-Check circuit for an input sequence of the data is;

$$RDS\max = \frac{\max}{0 \le n \le k} \left(\left| \sum_{i=0}^{n} (2x_i - 1) + RDS0 \right| \right),$$

wherein the flip bit is inserted after k input bits.

31. The disk drive of Claim 19 wherein the DC-Check circuit includes limiting a maximum DC offset of a filtering operation.

32. The disk drive of Claim 31 wherein the DC-Check circuit includes a low pass filter having a transfer function that complements the filtering operation; and

an absolute value determiner to determine an absolute value of an output of the low pass filter.

33. The disk drive of Claim 19 wherein the DC-Check circuit includes limiting for a DC correction circuit.

34. The disk drive of Claim 33 wherein the DC-Check circuit includes a low pass filter to model the DC correction circuit; and

an offset estimation filter.

35. The disk drive of Claim 19 wherein the DC-Check circuit includes threshold limiting.

36. A method of encoding a communication signal, comprising:

buffering data associated with the communication signal;

computing a metric as a function of the data;

generating a flip signal as a function of the metric, the flip signal having a flip state and a nonflip state; and

responsive to the flip signal, controlling a flip bit of the data such that an average DC value of the data approaches zero.

37.   The method of Claim 36 wherein the computing the metric includes;

providing at least two DC-Check circuits including a first DC-Check circuit and a second DC-Check circuit;

initializing the at least two DC-Check circuits;

inserting a zero before a new codeword of the data;

buffering the new codeword;

generating words in each of the DC-Check circuits; and

selecting a winning word of the words.

38.   The method of Claim 37 wherein the initializing includes;

determining whether the data is prior to a first codeword;

for data prior to the first codeword;

a) passing the data through the first DC-Check circuit;

   b)   setting a state of the second DC-Check

circuit to a state of the first DC-Check circuit.

39.   The method of Claim 36 wherein the controlling the

flip bit includes;

   if the winning word is from the first DC-Check circuit;

      setting the state of the first DC-Check circuit to

the state of the second DC-Check circuit; and

      passing an inverse of the new codeword to the

output; and

   if the winning word is from the second DC-Check circuit;

      setting the state of the second DC-Check circuit to

the state of the first DC-Check circuit; and

      passing the new codeword to the output.

40.   The method of Claim 37 further comprising precoding

the new codeword.

41.   The method of Claim 36 wherein the metric is

selected from a group consisting of a maximum absolute value

of a running digital sum of the data, a maximum DC offset

introduced by a filtering operation, a maximum DC offset of a

DC correction circuit, a maximum absolute value of a filtered

output of the data, a maximum DC offset slope change of the

running digital sum of the data, a count of the quantity of times the metric is above or below a threshold, and combinations thereof.

42. The method of Claim 36 wherein the data includes past encoder outputs and possible future encoder outputs.

43. The method of Claim 36 wherein the flip bit is at least two flip bits.

44. The method of Claim 36 further comprising inserting the flip bit after every k input bits of the data.

45. The method of Claim 36 further comprising providing two DC-Check circuits corresponding to each flip bit.

46. The method of Claim 36 wherein the metric includes limiting a maximum of an absolute value of a running digital sum.

47. The method of Claim 46 wherein the running digital sum up to time n is defined as;

$$RDS(T_0, n) = \sum_{i=T_0}^{n} (2x_i - 1), where (-\infty < T_0 < 0),$$

RDS(T_0,n)=RDS(T_o,-1)+RDS(0,n) and,

RDS0=RDS(T_o,-1),

where x_i represents encoder outputs, and RDS0 is a state of a DC-Check circuit before new data is entered.

48. The method of Claim 47 wherein an output of the DC-Check circuit for an input sequence of the data is;

$$RDS\max = \mathop{\max}_{0 \le n \le k} \left(\left| \sum_{i=0}^{n} (2x_i - 1) + RDS0 \right| \right),$$

wherein the flip bit is inserted after k input bits.

49. The method of Claim 36 wherein the metric includes limiting a maximum DC offset of a filtering operation.

50. The method of Claim 49 further comprising providing a DC-Check circuit including a low pass filter having a transfer function that complements the filtering operation; and

an absolute value determiner to determine an absolute value of an output of the low pass filter.

51. The method of Claim 36 wherein the metric includes limiting for a DC correction circuit.

52. The method of Claim 51 further comprising providing a DC-Check circuit including a low pass filter to model the DC correction circuit; and

an offset estimation filter.

53. The method of Claim 36 wherein the metric includes threshold limiting.

54. An encoder to encode a communication signal, comprising:

means for buffering to buffer data associated with the communication signal;

means for metric computing to compute a metric as a function of the data;

means for DC tracking to generate a flip signal as a function of the metric, the flip signal having a flip state and a nonflip state; and

means for flipping, responsive to the flip signal, to control a flip bit of an output of the buffering means such that an average DC value of the data approaches zero.

55. The encoder of Claim 54 wherein the metric is selected from a group consisting of a maximum absolute value of a running digital sum of the data, a maximum DC offset

introduced by a filtering operation, a maximum DC offset of a

DC correction circuit, a maximum absolute value of a filtered

output of the data, a maximum DC offset slope change of the

running digital sum of the data, a count of the quantity of

times the metric is above or below a threshold, and

combinations thereof.

56.   The encoder of Claim 54 further comprising means for

precoding to generate the data from the communication signal.

57.   The encoder of Claim 54 wherein the data includes

sectors; and

the metric being a function of the data sectors.

58.   The encoder of Claim 54 wherein the data includes

codewords; and

the metric being a function of the data codewords.

59.   The encoder of Claim 54 wherein the data includes

past encoder outputs and possible future encoder outputs.

60.   The encoder of Claim 54 wherein the flip bit is at

least two flip bits.

61. The encoder of Claim 54 wherein the flip bit is inserted after every k input bits of the data.

62. The encoder of Claim 54 wherein there are two means for metric computing corresponding to each flip bit.

63. The encoder of Claim 54 wherein the means for metric computing includes limiting a maximum of an absolute value of a running digital sum.

64. The encoder of Claim 63 wherein the running digital sum up to time n is defined as;

$$RDS(T_0, n) = \sum_{i=T_0}^{n} (2x_i - 1), where(-\infty < T_0 < 0) ,$$

RDS(T_0,n) =RDS(T_0,-1)+RDS(0,n) and,

RDS0=RDS(T_0,-1),

where x_i represents encoder outputs, and RDS0 is a state of the metric computing means before new data is entered.

65. The encoder of Claim 64 wherein an output of the metric computing means for an input sequence of the data is;

$$RDS\max = \frac{\max}{0 \leq n \leq k} \left(\left| \sum_{i=0}^{n} (2x_i - 1) + RDS0 \right| \right) ,$$

wherein the flip bit is inserted after k input bits.

66. The encoder of Claim 54 wherein the metric computing means includes limiting a maximum DC offset of a filtering operation.

67. The encoder of Claim 66 wherein the metric computing means includes means for low pass filtering having a transfer function that complements the filtering operation; and

an absolute value determiner to determine an absolute value of an output of the means for low pass filtering.

68. The encoder of Claim 54 wherein the metric computing means includes limiting for a DC correction circuit.

69. The encoder of Claim 68 wherein the metric computing means includes means for filtering to model the DC correction circuit; and

an offset estimation filter.

70. The encoder of Claim 54 wherein the metric computing means includes threshold limiting.

71. A disk drive comprising:

means for signal processing to process a perpendicular recording input signal;

a DC-free encoder to generate an encoded signal as a function of the perpendicular recording input signal, the DC-free encoder including;

means for buffering to buffer data associated with the perpendicular recording input signal;

means for metric computing to compute a metric as a function of the data;

means for DC tracking to generate a flip signal as a function of the metric, the flip signal having a flip state and a nonflip state; and

means for flipping, responsive to the flip signal, to control a flip bit of an output of the buffering means such that an average DC value of the data approaches zero;

means for preamplifying to transmit the encoded signal; and

media to store the encoded signal as first data.

72. The disk drive of Claim 71 further including a read head amplifier to read the first data from the media;

means for DC-free decoding to decode the first data; and

the signal processing means to generate an output signal as a function of the decoded first data.

73. The disk drive of Claim 72 wherein the metric is selected from a group consisting of a maximum absolute value of a running digital sum of the data, a maximum DC offset introduced by a filtering operation, a maximum DC offset of a DC correction circuit, a maximum absolute value of a filtered output of the data, a maximum DC offset slope change of the running digital sum of the data, a count of the quantity of times the metric is above or below a threshold, and combinations thereof.

74. The disk drive of Claim 72 further comprising means for precoding to generate the data from the communication signal.

75. The disk drive of Claim 72 wherein the data includes sectors; and

the metric being a function of the data sectors.

76. The disk drive of Claim 72 wherein the data includes codewords; and

the metric being a function of the data codewords.

77. The disk drive of Claim 72 wherein the data includes past encoder outputs and possible future encoder outputs.

78. The disk drive of Claim 72 wherein the flip bit is at least two flip bits.

79. The disk drive of Claim 72 wherein the flip bit is inserted after every k input bits of the data.

80. The disk drive of Claim 72 wherein there are two means for metric computing corresponding to each flip bit.

81. The disk drive of Claim 72 wherein the means for metric computing includes limiting a maximum of an absolute value of a running digital sum.

82. The disk drive of Claim 81 wherein the running digital sum up to time n is defined as;

$$RDS(T_0, n) = \sum_{i=T_0}^{n} (2x_i - 1), where (-\infty < T_0 < 0),$$

RDS (T_0, n) =RDS $(T_o, -1)$ +RDS $(0, n)$ and,

RDS0=RDS $(T_o, -1)$,

where x_i represents encoder outputs, and RDS0 is a state of the means for metric computing before new data is entered.

83. The disk drive of Claim 82 wherein an output of the means for metric computing for an input sequence of the data is;

$$RDS\max = \frac{\max}{0 \le n \le k} \left(\left| \sum_{i=0}^{n} (2x_i - 1) + RDS0 \right| \right),$$

wherein the flip bit is inserted after k input bits.

84. The disk drive of Claim 72 wherein the means for metric computing includes limiting a maximum DC offset of a filtering operation.

85. The disk drive of Claim 84 wherein the means for metric computing includes means for low pass filtering having a transfer function that complements the filtering operation; and

an absolute value determiner to determine an absolute value of an output of the means for low pass filtering.

86. The disk drive of Claim 72 wherein the means for metric computing includes limiting for a DC correction circuit.

87. The disk drive of Claim 86 wherein the means for metric computing includes means for low pass filtering to model the DC correction circuit; and

an offset estimation filter.

88. The disk drive of Claim 72 wherein the means for metric computing includes threshold limiting.

89. A computer program to configure a general purpose computer to perform a method for encoding a communication signal, comprising:

buffering data associated with the communication signal;

computing a metric as a function of the data;

generating a flip signal as a function of the metric, the flip signal having a flip state and a nonflip state; and

responsive to the flip signal, controlling a flip bit of the data such that an average DC value of the data approaches zero.

90. The computer program of Claim 89 wherein the computing the metric includes;

providing at least two DC-Check circuits including a first DC-Check circuit and a second DC-Check circuit;

initializing the at least two DC-Check circuits;

inserting a zero before a new codeword of the data;

buffering the new codeword;

generating words in each of the DC-Check circuits; and

selecting a winning word of the words.

91. The computer program of Claim 90 wherein the

initializing includes;

determining whether the data is prior to a first

codeword;

for data prior to the first codeword;

a) passing the data through the first DC-Check

circuit;

b) setting a state of the second DC-Check

circuit to a state of the first DC-Check circuit.

92. The computer program of Claim 89 wherein the

controlling the flip bit includes;

if the winning word is from the first DC-Check circuit;

setting the state of the first DC-Check circuit to

the state of the second DC-Check circuit; and

passing an inverse of the new codeword to the

output; and

if the winning word is from the second DC-Check circuit;

setting the state of the second DC-Check circuit to

the state of the first DC-Check circuit; and

passing the new codeword to the output.

93. The computer program of Claim 90 further comprising

precoding the new codeword.

94. The computer program of Claim 89 wherein the metric

is selected from a group consisting of a maximum absolute

value of a running digital sum of the data, a maximum DC

offset introduced by a filtering operation, a maximum DC

offset of a DC correction circuit, a maximum absolute value of

a filtered output of the data, a maximum DC offset slope

change of the running digital sum of the data, a count of the

quantity of times the metric is above or below a threshold,

and combinations thereof.

95. The computer program of Claim 89 wherein the data

includes past encoder outputs and possible future encoder

outputs.

96. The computer program of Claim 89 wherein the flip

bit is at least two flip bits.

97. The computer program of Claim 89 further comprising inserting the flip bit after every k input bits of the data.

98. The computer program of Claim 89 further comprising providing two DC-Check circuits corresponding to each flip bit.

99. The computer program of Claim 89 wherein the metric includes limiting a maximum of an absolute value of a running digital sum.

100. The computer program of Claim 99 wherein the running digital sum up to time n is defined as;

$$RDS(T_0, n) = \sum_{i=T_0}^{n} (2x_i - 1), where(-\infty < T_0 < 0),$$

RDS(T₀,n) =RDS(T₀,-1)+RDS(0,n) and,

RDS0=RDS(T₀,-1),

where x_i represents encoder outputs, and RDS0 is a state of a DC-Check circuit before new data is entered.

101. The computer program of Claim 100 wherein an output of the DC-Check circuit for an input sequence of the data is;

$$RDS\max = \frac{\max}{0 \leq n \leq k} \left(\left| \sum_{i=0}^{n} (2x_i - 1) + RDS0 \right| \right),$$

wherein the flip bit is inserted after k input bits.

102. The computer program of Claim 89 wherein the metric includes limiting a maximum DC offset of a filtering operation.

103. The computer program of Claim 102 further comprising providing a DC-Check circuit including a low pass filter having a transfer function that complements the filtering operation; and

an absolute value determiner to determine an absolute value of an output of the low pass filter.

104. The computer program of Claim 89 wherein the metric includes limiting for a DC correction circuit.

105. The computer program of Claim 104 further comprising providing a DC-Check circuit including a low pass filter to model the DC correction circuit; and

an offset estimation filter.

106. The computer program of Claim 89 wherein the metric includes threshold limiting.